Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A single instruction, multiple data (SIMD) controller for processing a plurality of data streams in a digital subscriber line (DSL) system, comprising:

a plurality of circular buffer circuits ~~coupled to~~ that store data from said plurality of data streams;

a plurality of address generation circuits ~~coupled to~~ that access said data stored in said plurality of circular buffer circuits;

a plurality of processor circuits ~~coupled to~~ that process said data accessed by said plurality of address generation circuits; and

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a program control unit ~~coupled to control~~ that controls said plurality of processor circuits with an instruction.

2. (Currently amended) The controller of claim 1, wherein one of said plurality of circular buffer circuits comprises:

a first section ~~coupled to store~~ that stores one or more symbols before being processed;

a second section ~~coupled to store~~ that stores said one or more symbols being processed; and

a third section ~~coupled to store~~ that stores said one or more symbols after being processed.

3. (Currently amended) The controller of claim 1, wherein one of said plurality of address generation circuits comprises:

a symbol manager circuit ~~coupled to generate~~ that generates an input base address, a processor base address, and an output base address,

wherein said one of said plurality of address generation circuits ~~is~~ further ~~coupled to receive~~ receives an input offset address, a processor offset address, and an output offset address, and ~~to generate~~ generates an input address, a processor address, and an output address in accordance with said input base address, said processor base address, and said output base address.

4. (Currently ~~amended~~) The controller of claim 1, wherein said plurality of processor circuits ~~are~~ further ~~coupled to~~ receive a plurality of enable signals and ~~to~~ selectively process said data based on said plurality of enable signals.

5. (Currently amended) The controller of claim 1, wherein said plurality of address generation circuits ~~are~~ further ~~coupled to~~ selectively generate a plurality of enable signals, depending upon whether a full symbol is ready for processing in each of said plurality of address generation circuits.

6. (Currently amended) The controller of claim 5, wherein said plurality of processor circuits ~~are~~ further ~~coupled to~~ receive said plurality of enable signals and ~~to~~ selectively process said data based on said plurality of enable signals.

7. (Currently amended) The controller of claim 1, wherein said plurality of address generation circuits ~~are~~ further ~~coupled to~~ selectively generate a plurality of enable signals, depending upon a difference between an input base address and a processor base address in each of said plurality of address generation circuits.

8. (Original) A method of processing a plurality of data streams in a digital subscriber line (DSL) system, comprising the acts of:

calculating a plurality of input addresses for said plurality of data streams based on a plurality of input base addresses and a plurality of input offset addresses;

storing a plurality of data from said plurality of data streams according to said plurality of input addresses;

calculating a plurality of processor addresses for the stored plurality of data based on a plurality of processor base addresses and a plurality of processor offset addresses;

processing, using a single instruction, the stored plurality of data according to said plurality of processor addresses;

calculating a plurality of output addresses for the processed plurality of data based on a plurality of output base addresses and a plurality of output offset addresses;

outputting the processed plurality of data according to said plurality of output addresses; and

updating said plurality of input base addresses, said plurality of processor base addresses, and said plurality of output base addresses.

9. (New) A single instruction, multi data (SIMD) architecture for controlling the processing of plurality of data streams, comprising:

a memory that stores data from said plurality of data streams received from a plurality of channels;

a processor, operatively coupled with said memory, that processes said data from said plurality of data streams; and

a controller that controls said processor,

wherein storing said data in said memory de-couples a first operating rate of said processor and a second operating rate of said plurality of channels.

10. (New) A SIMD architecture as defined in claim 9, wherein said plurality of data streams are carried in respective ones of said plurality of channels.

11. (New) A method of controlling processing of multiple data streams in a single instruction, multi data (SIMD) architecture, comprising the steps of:

storing data in a memory as said data is received;

at regular intervals, determining whether all of said data has been received;

providing a signal indicating that all of said data has been received;

using said signal to determine which of said data to process; and

processing said data in accordance with said signal.

12. (New) A method as defined in claim 11, wherein said multiple data streams are carried in respective ones of a plurality of channels.